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D4T systems concludes with test automation tool suite in a successful EU project: TOETS

Overview

D4T Systems concluded with impressive results on pre-silicon IC test tool development in the three year lasting EU project named TOETS. TOETS is a Catrene initiative lead by NXP Semiconductors which aims to reduce IC test cost and time to market wrt cost of goods sold for semiconductor companies. High competition in this market urged the industry to combine efforts and to come to a unified approach for semiconductor testing. TOETS which is the acronym for **T**owards **O**ne **E**uropean **T**est **S**olution, aims to fulfil these goals. D4T Systems has participated in this program by contributing to pre-silicon test validation and test automation tools for IC production testing.

Key contributions D4T Systems to TOETS.

- Standardized test definition and protocol for common analog IC test. Set specification and instrument protocols.
  Contributing partners: Infineon, Atmel, Salland Engineering and D4T Systems (Lead).
- Implementation and pilot demonstration of instrument model database using standardized test definitions from previous milestone.
  Contributing partners: Salland Engineering and D4T Systems.
- Full automated test validation flow demonstration from design to tester using D4T Systems newly developed tool suite.
  Contributing partners: NXP, Atmel, Salland Engineering and D4T Systems.

Introduction to TOETS milestones

D4T Systems engaged primarily in time-to-market and cost reduction in the Analog Mixed-Signal (AMS) domain by means of the test development flow automation. The instrumental part in this task is an original tool suite that allows pre-silicon validation of an IC embedded in a tester environment. D4T Systems managed to complete the development of the tool suite named ***fanTESTic*** throughout the project period through the in-house knowledge and skills as well as through the fruitful cooperation with other partners within the project.

Work Overview

Main target set at the beginning of the TOETS project is the pre-silicon test development time and cost reduction for AMS circuits. The initial conditions for the tool suite development have been established within the first milestone on standardized test definition and protocols in conjunction with other partners (ATMEL, Salland, Infineon). This first result specified the requirements for standard AMS test language and is used as foundation for the D4T System's tool suite development.

The basic feature of the tool suite is the pre-silicon test validation through the simulation of an AMS test with all parameters required for the test platforms as agreed within this AMS standard test language. The tool achieves this through automatic test-bench generation, allowing real-time simulation of a test as if it were running on a tester. The screenshot of the tool is given in Figure 1. Test stimuli generation and post-processing capabilities for a number of mixed-signal blocks are developed and coupled with a GUI in

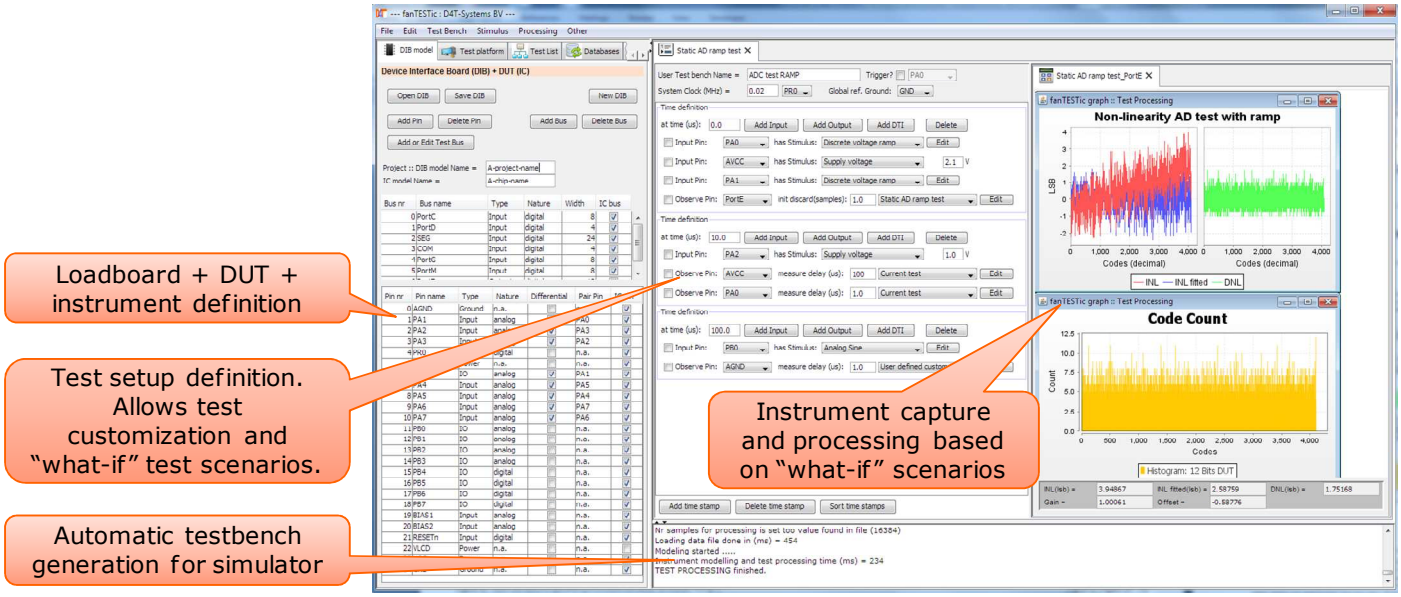

FIGURE 1: FANTESTIC TOOLSUITE SCREENSHOT

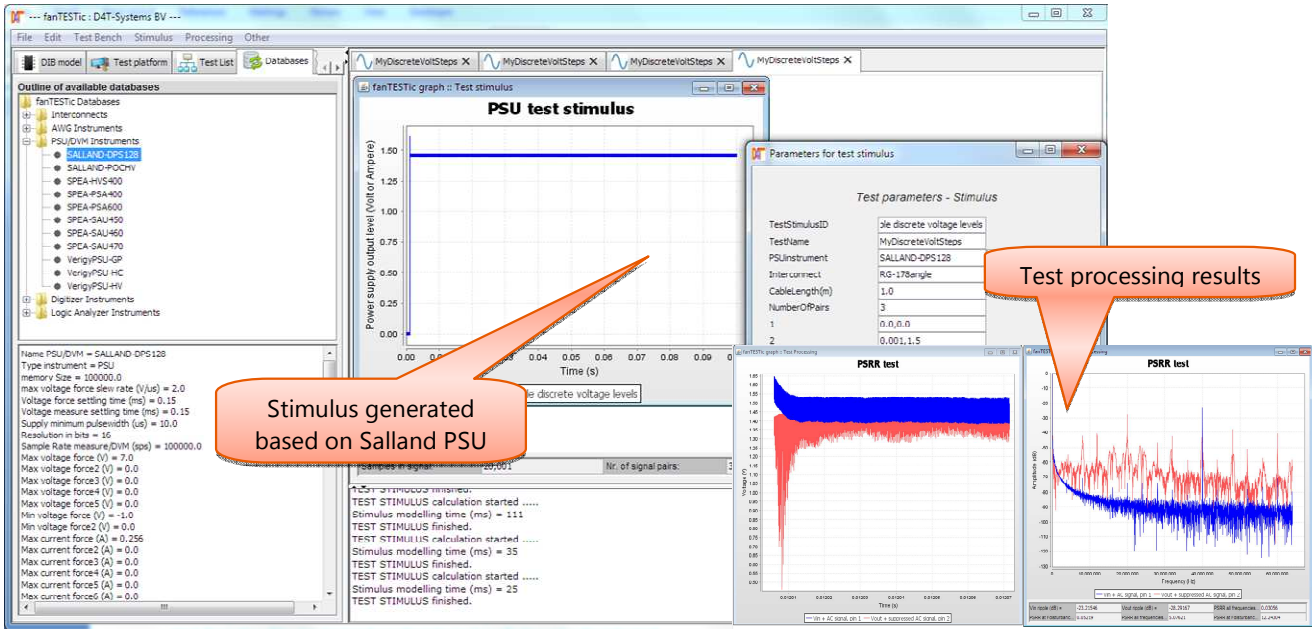

FIGURE 2: USING SALLAND'S PSU INSTRUMENTS FOR TEST SETUP VALIDATION IN FANTESTIC

Pre-silicon test analysis and validation tooling.

The early tool development effort has demonstrated the potentials within the next milestone for pilot demonstration with the cooperation of Salland. Salland's PSU instruments specification has been implemented as a model in D4T Systems tool database. These models are used to find an optimal test setup for a Power Supply Rejection Ratio (PSRR) test of a low noise amplifier in the front-end of an imaging Array in 130 nm technology (Figure 2)

Finally, the last milestone has demonstrated the additional value of the tool in bridging the gap between the design and test realms. In cooperation with Atmel, Salland and NXP, the D4T tool suite has carried out the test synthesis flow and linked the test specification from design database to the capabilities of tester platforms. This flow is used to find the optimal test setup in terms of costs, while at the same time reducing significantly the test development time. Figure 1 demonstrates this full test flow demonstration for the test setup on an Atmel ADC which is part of a larger microcontroller chip (ATxmega series).

- Test program development time:
  - development time per critical and per sub test function
  - developed by DFT/test development engineer
- Test debug time
  - all tests require debugging to ensure correctness
  - nr. of tests in % and time needed in hrs defined per debug category: hard/medium/easy + time needed for each category (tester, engineer, operator).
- Model applied to both the traditional way of working and the new simulation tool based way of working. The model weights the average use of tester and development hours for the phases of development and debug.

Quantification D4T Systems when using their test simulation and validation tool		
savings on test program debug	55.7% savings in hours	55.7% cost saving (euro)
savings on test program development	11.0% savings in hours	11.0% cost saving (euro)
overall savings using pre-Si validation	***39.5% time reduction or gain in TTM***	***44.5% cost reduction***

Quantification – Added business value

Assuming the test program development time and test debug time as the two major factors adding to the overall time and costs, D4T systems quantification business model is shown to be as follows:

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