European Library-based flow of Embedded Silicon test Instruments

ELESIS final review
December 2015

Goal & Technology

Goal: Tools to support methods for qualifying dependability sensors IP in System-On-Chip

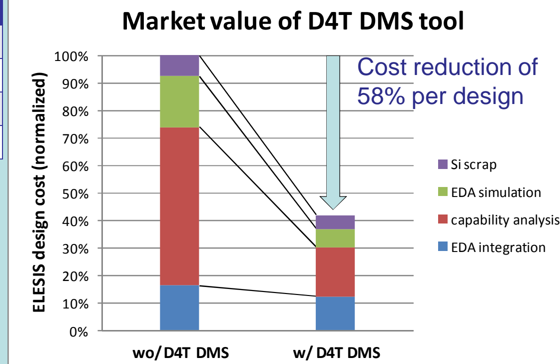
Method: New software comprising a model driven, statistical simulation approach with build-in dependability IP database.

A tool to assess the quality and sustained performance of SoC's over operational lifetime

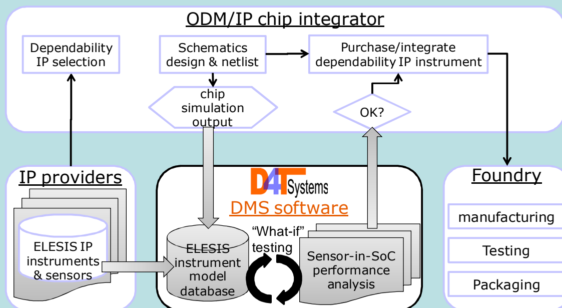
Dependability Model Simulator - DMS

ELESIS exploitation & KPI's: connecting project targets to customer key benefits with new DMS tool

DMS: customer key benefit	ELESIS KPI
Reduced **EDA integration time** for dependability features.	TIME
Advanced **sensor-in-SoC capability analysis** due to accurate model database	QUALITY
Reduced "what-if" simulation effort for dependability IP in SoC	TIME
Reduced wafer and silicon waste by more efficient IP debug	COST



D4T Systems DMS tool is positioned at the pre-silicon design phase.



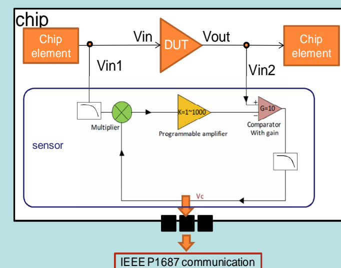
ELESIS technology results: DMS software demonstration of dependability IP evaluation on AMS DUT

Dependability Model Simulator demo:

Capability analysis on ELESIS sensor to monitor DC drift due to aging in SoC IP.

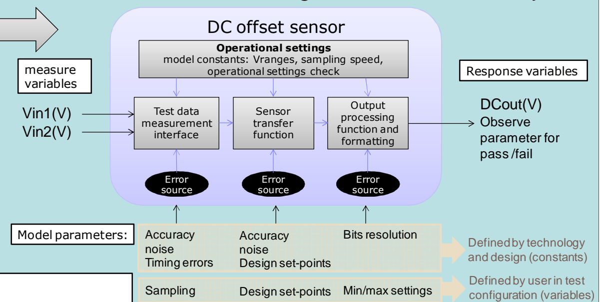
This dependability IP is evaluated on two devices with DMS:
1) General purpose OpAmp IP block for SoC's
2) High grade, robust OpAmp IP for SerDes high speed communication.

From transistor level circuit simulation to .....



Dependability sensor:
1) DC offset drift due to NBTI.
2) DC offset sensed from AC signals through gain optimized loop

Model based design with statistical analysis



IP model database

Workbench: sensor test and simulation setup

Database with libraries. The ELESIS instruments are implemented for two variants

The datasheet parameters as they will be used in the sensor model

User defined variables are defined and can vary per test

Analysis: capability of dependability IP in SoC

DMS analysis output. Detected DC drift is displayed with statistical boundaries.

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For product pricing, services and technical information, please contact:
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