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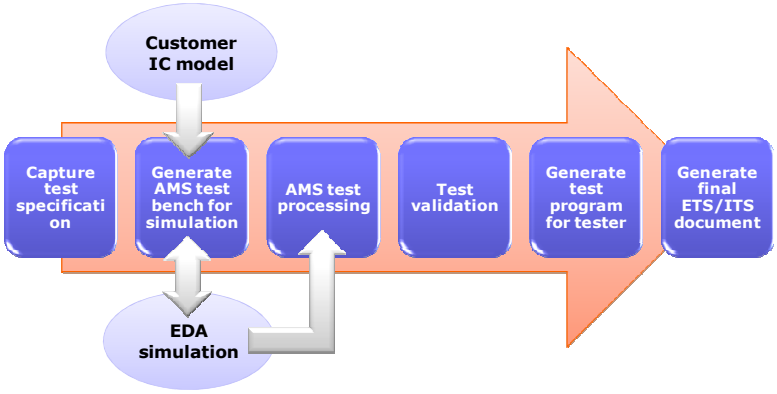
fanTESTic — Analog Mixed Signal Test Automation and Simulation

Overview fanTESTic

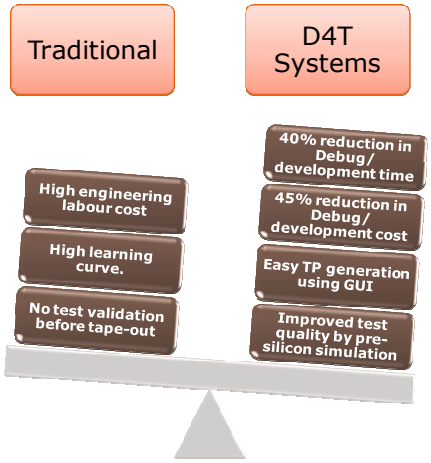
fanTESTic is the industry's most comprehensive software tool dedicated to analog mixed signal circuits (AMS) for simulation, validation and generation of test plans for tester platforms. It simulates an AMS test with all the parameters required for a test platform. Now, simulating a test as if it was running on the tester is within your reach. The tool facilitates quick development of the test program process. Annoying test debug times are significantly reduced by using the tool. fanTESTic enables test engineers to simulate tests without designers knowledge, reduce their test development time and improve on fast customer delivery, time-to-market and test quality.



Key benefits and features of fanTESTic.

- fanTESTic's pre-silicon verification flow reduces test development plus debug time with 40%.
- fanTESTic brings about 45% cost reduction in the test development and debug phase, depending on project complexity.
- Automatic test bench generation validated by tester specific simulation.
- Easy and user friendly graphical user interface.
- Extensive model database for most tester instrument vendors and cable-connector interfaces.
- No HDL knowledge needed, fanTESTic generates all required code.
- Closed loop test engineering, verification by simulation and porting to tester input program.
- Built-in test library for common test functions.
- Custom test development based on a wide range of standard test stimuli.
- Compatible with virtually any EDA environment or ATE platform.

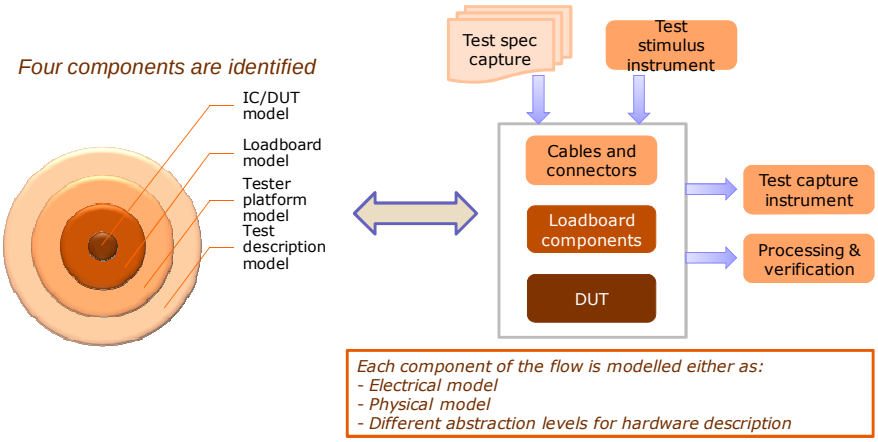
fanTESTic solves all the major issues that are encountered when developing a test program for your tester platform. Test simulation with tester specific parameters integrates effectively



the test cycle into the design cycle. The AMS test is simulated as if it were running on your test system. An easy to use GUI supports the capture of the test specification.

fanTESTic Technology

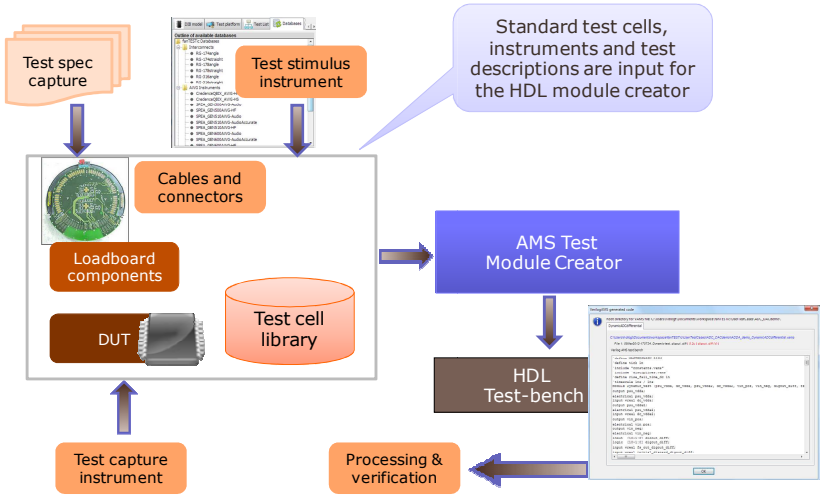
fanTESTic is based on model driven test development and identifies four basic models in the test flow: 1) Test description, 2) Test instrument, 3) load-board, 4) IC. The tool incorporates a model for every instance required in the test engineering process. Meaning, a large database of commercial test instruments and test platforms are available as model. These models incorporate the tester specific behaviour and are used in the test simulation. On top of that, the tool accommodates interconnectivity models for cables and connectors as well as a fully UI driven test bench description approach with pre-defined tests.
fanTESTic runs on modern JAVA based technology. The state-of-the-art core technology enables high and easy integration within virtually all modern platform technologies.



The enabling core technology is based on a complete solution for capturing the test specification, automatically generating the HDL code for simulation and the test program input for the tester. External input requirements are

- A model of the device under test (DUT). This can be a Verilog.(AMS) model, transistor level design or a combination of both.
- EDA simulator compatible with the Verilog.AMS standard.

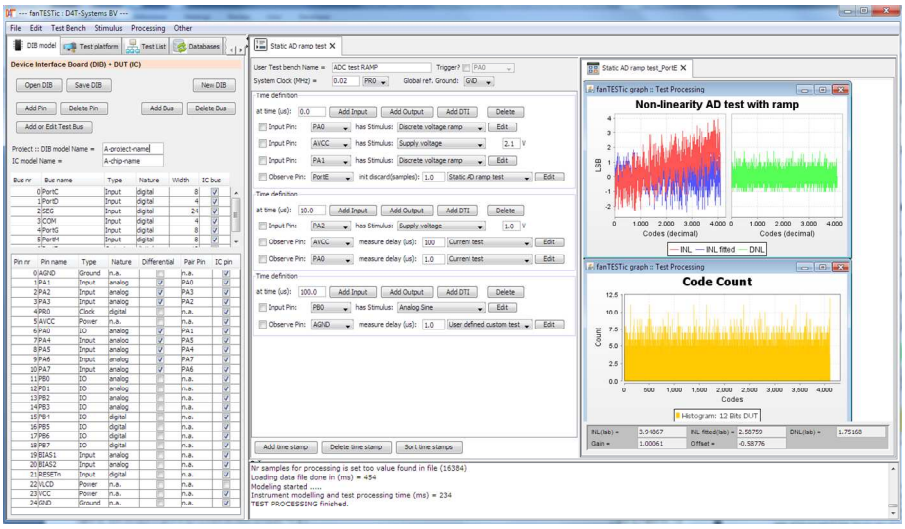
Without HDL models, the user can still take advantage of the benefits of fanTESTic. A full transistor level design is easily accepted by the tool if the user is willing to accept longer computation times. fanTESTic's post-processor typically includes an FFT for estimating distortion components and noise levels. Histogram testing and non linearity testing are supported as well.



Powerful test-into-design integration

Key is the integration of the test development cycle into the design cycle. Now, test engineers are offered the benefits of design simulation without the burden of needing the knowledge of the full complex EDA environment. fanTESTic is dedicated to the test domain simulation of the design. Therefore the test engineer can stay committed to his test task. Simulator knowledge is not required.

Capturing the test specification is supported by the comprehensive GUI which eases the task by delivering predefined parameter input sections to the user. The test bench is automatically generated from the users test



specification by a push button approach and can directly be used in the EDA simulator. The test bench for the simulator is an HDL standard, based on Verilog.AMS. Verilog and Verilog.AMS are widely used standards across design communities worldwide and allow for easy integration into the EDA environment. Test output response will be calculated by the powerful post-processing features of fanTESTic. No post processing steps from the EDA environment need to be invoked by the user. FFT analysis and statistical non-linearity calculations are supported for the most common set of AMS testing e.g. for AD and DA convertors. But also directly captured responses from DUT pins can be viewed in the GUI and used in test limit comparison. Once satisfied with the simulation outcome of the test-plan, the tool will generate the template code for execution on the tester platform. Due to closed loop engineering with simulation, the debug and development time will decrease dramatically thereby also increasing the test quality.

From simulation to tester

Simulation now becomes a very powerful mechanism for a test engineer to quickly verify the output response of his test plan. Key is the correct simulation of the test and test set-up as is defined by the performance characteristics of the tester platform. For example, fanTESTic takes into account sampling frequencies, resolutions, triggers and coherency calculations. Virtually the whole test setup is verified including loadboard models for connectivity with active/passive elements. This is a huge benefit of the tool, differentiating it from the common EDA solutions which target to verify design performance. Limitations in accuracy of the tester platform can be modeled with the fanTESTic test flow.

Formats and interfaces

Supported formats for the DUT:
Verilog, Verilog.AMS, transistor netlist

Simulator and EDA support
Verilog.AMS must be supported by the simulator or EDA provider

Platform & Environments
Linux/UNIX/PC-Windows
JAVA server

Summary

fanTESTic is provided by D4T systems as a tool to speed up the test development cycle and decrease the test debug time on mixed signal circuits. The modern technology enables test engineering to verify already at pre-silicon the test plan using models in simulation. Subsequently, the verified test plan is ported to most tester platforms for execution after compilation. fanTESTic offers improved Time-to-Market and test quality.

For more information on D4T systems products visit us at www.d4t-systems.com